

CLAIMS

1. A switching circuit comprising:

at least two switches coupled to an upper voltage and a lower voltage;

5 and ~~B3M~~

at least one passive break-before-make element coupled in series to the at

Fig. 3 least two switches; and

wherein the switching circuit is coupled to a load.

2. The switching circuit of claim 1, further comprising:

10 a low pass filter, wherein the switching circuit is coupled to the load
through the low pass filter.

3. The switching circuit of claim 1, wherein the passive break-before-make
Fig. 7 element comprises:

a resistive element and an inductive element coupled in parallel.

15 4. The switching circuit of claim 1, wherein the passive break-before-make
element comprises:

Fig. 8 a resistive element and a capacitive element coupled in series; and
an inductive element coupled in parallel to the resistive element and the
capacitive element.

5. The switching circuit of claim 2, wherein the low pass filter includes at least one inductor and at least one capacitor.
6. The switching circuit of claim 1, wherein the switching circuit is included in a push-pull circuit configuration.
7. The switching circuit of claim 1, wherein the at least two switches are transistors.
8. The switching circuit of claim 1, wherein the switching circuit is internal to an integrated circuit chip.

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9. A switching circuit comprising:

at least two switches coupled to an upper voltage and a lower voltage;

and

MBB

Fig. 9

at least one passive make-before-break element coupled in parallel to the

at least two switches; and

wherein the switching circuit is coupled to a load.

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10. The switching circuit of claim 9, further comprising:

a low pass filter, wherein the switching circuit is coupled to the load

through the low pass filter.

11. The switching circuit of claim 9, wherein the passive make-before-break element comprises:

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a resistive element and a capacitive element coupled in series.

12. The switching circuit of claim 10, wherein the low pass filter includes at least one inductor and at least one capacitor.

13. The switching circuit of claim 9, wherein the switching circuit is included in a push-pull circuit configuration.

5 14. The switching circuit of claim 9, wherein the at least two switches are transistors.

15. The switching circuit of claim 9, wherein the switching circuit is internal to an integrated circuit chip.

16. A switching audio amplifier circuit comprising:

10 a digital circuit providing a switching signal;

at least two switches coupled to an upper voltage and a lower voltage for

receiving the switching signal; and

at least one passive break-before-make^{B/M} element coupled in series to the at

least two switches; and

15 wherein the switching audio amplifier circuit is coupled to a load through a low pass filter.

17. The switching audio amplifier circuit of claim 16, wherein the load is a speaker system.

18. The switching audio amplifier circuit of claim 16, wherein the passive break-before-make element comprises:

a resistive element and an inductive element coupled in parallel.

19. The switching audio amplifier circuit of claim 16, wherein the passive break-before-make element comprises:

a resistive element and a capacitive element coupled in series; and

an inductive element coupled in parallel to the resistive element and the

5 capacitive element.

20. The switching audio amplifier circuit of claim 16, wherein the switching audio amplifier circuit is included in a push-pull circuit configuration.

21. A switching audio amplifier circuit comprising:

a digital circuit providing a switching signal;

10 at least two switches coupled to an upper voltage and a lower voltage for receiving the switching signal; and

at least one passive ^{MBB} make-before-break element coupled in parallel to the at least two switches; and

15 wherein the switching audio amplifier circuit is coupled to a load through a low pass filter.

22. The switching audio amplifier circuit of claim 21, wherein the load is a speaker system.

23. The switching audio amplifier circuit of claim 21, wherein the passive make-before-break element comprises:

20 a resistive element and a capacitive element coupled in series.

24. The switching audio amplifier circuit of claim 21, wherein the switching audio amplifier circuit is included in a push-pull circuit configuration.

25. A method for operation of a switching circuit, comprising:
applying a switching signal to the switching circuit; and
5 providing a passive break-before-make element in the switching circuit;
and
wherein the passive break-before-make element provides a high
impedance in a short term and a low impedance in a long term.

26. The method of claim 25, wherein the passive break-before-make element
10 includes a storage element, the method further comprising:
storing excess energy during a switching transition of the switching
circuit in the storage element.

27. The method of claim 26, wherein the storage element is an inductive
element.

15 28. The method of claim 25, wherein the passive break-before-make element
includes a dissipation element, the method further comprising:
dissipating excess energy during a switching transition of the switching
circuit in the dissipation element.

20 29. The method of claim 28, wherein the dissipation element is a resistive
element.

30. A method for operation of a switching circuit, comprising:
applying a switching signal to the switching circuit; and
providing a passive make-before-break element in the switching circuit;
and

5 wherein the passive make-before-break element provides a high
impedance in a short term and a low impedance in a long term.

31. The method of claim 30, wherein the passive make-before-break element
includes a storage element, the method further comprising:
storing excess energy during a switching transition of the switching
10 circuit in the storage element.

32. The method of claim 31, wherein the storage element is a capacitive
element.

33. The method of claim 30, wherein the passive make-before-break element
includes a dissipation element, the method further comprising:
15 dissipating excess energy during a switching transition of the switching
circuit in the dissipation element.

34. The method of claim 33, wherein the dissipation element is a resistive
element.

35. A switching circuit having feedback, comprising:
20 a differential duty ratio adjuster (DDRA) having a first input to receive a
pulse width modulation (PWM) signal, a second input to receive a

reference voltage, and a third input to receive a first feedback signal,
wherein the DDRA comprises:

- a first digital gate having a first input to receive the PWM signal;
- a first duty ratio modulator having a first input to receive the PWM
5 signal and a second input to receive the first feedback signal;
and
- a second digital gate having a first input to receive an output of the
first duty ratio modulator.

36. The switching circuit of claim 35, further comprising an error amplifier
10 coupled to the DDRA and having a first output to provide the first
feedback signal to the DDRA.

37. The switching circuit of claim 36, further comprising:

- a power stage having an input to receive an output of the second digital
gate; and

- 15 a summing node having a first input to receive an output of the power
stage and a second input to receive an output of the first digital gate,
wherein the summing node provides a difference to the error
amplifier.

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43. The switching circuit of claim 42, wherein:

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44. The switching circuit of claim 42, wherein the second resistor and capacitor slows down edge transitions of the PWM signal and introduces a time delay into the PWM signal.
45. The switching circuit of claim 44, wherein the first digital gate converts the
5 output of the first duty ratio modulator to a digital signal.
46. The switching circuit of claim 38, wherein the first duty ratio modulator and the second duty ratio modulator each further comprise a first resistor, a second resistor, and a capacitor, wherein:
the second resistor and capacitor of the first duty ratio modulator
10 introduces a time delay into the PWM signal, and
the second resistor and capacitor of the second duty ratio modulator compensates for the time delay.
47. The switching circuit of claim 46, wherein second resistor and capacitor of the second duty ratio modulator further compensates for a time delay of the
15 power stage.
48. The switching circuit of claim 35, wherein the switching circuit is internal to an integrated circuit.
49. The switching circuit of claim 35, wherein:
the first digital gate has a second input to receive the reference voltage;
20 and
the second digital gate has a second input to receive the reference voltage.

50. The switching circuit of claim 38, further comprising:

a third digital gate having a first input to receive the PWM signal, a second input to receive the reference voltage, and an output coupled to the second duty ratio modulator and the first duty ratio modulator, wherein the third digital gate removes noise from the PWM signal.

51. A method of providing feedback to a switching circuit having a power stage, comprising:

receiving a PWM signal;

adjusting the PWM signal to form a lower noise PWM signal;

modulating the PWM signal using feedback to form a corrected PWM signal;

providing the corrected PWM signal to the power stage to produce an amplified PWM signal; and

producing a feedback signal based at least in part on the amplified PWM signal and the lower noise PWM signal.

53. The method of claim 52, wherein modulating further comprises delaying the PWM signal.

54. The method of claim 53, wherein modulating the PWM signal uses at least two resistors and at least one capacitor.

55. The method of claim 53, wherein adjusting the PWM signal comprises delaying the PWM signal.

56. The method of claim 55, wherein delaying the PWM signal to form the lower noise PWM signal is performed to reduce the feedback signal.

57. The method of claim 51, wherein producing the feedback signal comprises calculating a difference between the lower noise PWM signal and the amplified PWM signal.

58. A switching circuit having feedback, comprising:

a differential duty ratio adjuster (DDRA) having a first input to receive a pulse width modulation (PWM) signal, a second input to receive a reference voltage, and a third input to receive a first feedback signal, wherein the DDRA comprises:

a first combinational logic circuit having an input for receiving the PWM signal and an output for providing a delayed PWM signal; and

a second combinational logic circuit having a first input for receiving the PWM signal, a second input for receiving a feedback signal, and an output for providing a modulated PWM signal, wherein the modulated PWM signal is modulated in response to the feedback signal.

59. The switching circuit of claim 58, wherein:

the second combinational logic circuit further comprises a first delay line having a first input to receive the PWM signal and coupled to provide a delay in the modulated PWM signal; and

the first combinational logic circuit comprises a second delay line having a first input to receive the PWM signal, wherein the second delay line provides a delay in the delayed PWM signal that is approximately equal to the delay in the modulated PWM signal.

60. The switching circuit of claim 59, wherein:

the second combinational logic circuit comprises a first latch coupled to the first delay line and having an output to provide the modulated PWM signal; and

5 the first combinational logic circuit comprises a second latch coupled to the second delay line and having an output to provide the delayed PWM signal.

61. The method of claim 59, wherein the first delay line includes a second

input based at least in part on the feedback signal, wherein the feedback

10 signal selectively modifies a duty ratio of the PWM signal to produce the modulated PWM signal.

62. The method of claim 61, wherein the second input is further based in part

on a reference voltage, wherein the reference voltage is used in part to

determine the delay of the modulated PWM signal.

15 63. The method of claim 62, wherein the second delay line includes a second

input for receiving the reference voltage, wherein the reference voltage is

used in part to determine the delay of the delayed PWM signal.